AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) A frequency divider comprising:

a sequence of divide stages coupled to selectively provide a plurality of different divide ratios;

at least one multiplexer coupled to selectively feed back [[the]] an output of at least one of the divide stages to an input of another of the divide stages earlier in the sequence of divide stages; and

a duty-cycle stage coupled to at least one of the divide stages to correct a duty cycle of an output of at least one of the divide stages having an odd divide ratio.

2. (Original) The frequency divider of claim 1 further comprising at least one input coupled to receive a programmable control signal indicating which of the plurality of different divide ratios to apply.

3. (Previously presented) The frequency divider of claim 1 further comprising an input to receive a signal to be divided and wherein respective ones of the divide stages include a clock input coupled to the signal to be divided.

4. (Canceled)

5. (Canceled)

6. (Previously presented) The frequency divider of claim 1, wherein the duty-cycle stage includes:

a first input to receive a first signal having an unbalanced duty cycle;

a second input to receive a second signal, wherein the second signal is a delayed version of the first signal; and

logic to generate a signal having a balanced duty cycle using the first signal and the second signal.

7. (Previously presented) The frequency divider of claim 1 wherein respective ones of the divide stages include an activation input coupled to receive an activation signal to selectively turn off one or more divide stages if the one or more divide stages are not used for a selected divide ratio.

8. (Previously presented) The frequency divider of claim 1 further including self-correction logic coupled to outputs of at least some of the divide stages to correct an abnormal state of the frequency divider.

9. (Previously presented) The frequency divider of claim 8 further including a latch circuit in at least one of the divider stages, the latch circuit including:

the self-correction logic; and

selection circuitry implementing the at least one multiplexer.

10. (Canceled)

11. (Currently amended) A frequency divider comprising:

a plurality of divide stages programmably coupled to provide a plurality of different divide ratios; and

wherein one or more of the divide stages is turned off when not used for a programmed divide ratio.

~~wherein respective ones of the divide stages include an activation input coupled to receive an activation signal to selectively turn off one or more of the respective divide stages if the one or more of the respective divide stages are not used for a selected divide ratio~~.

12. (Previously presented) The frequency divider of claim 11 further comprising at least one multiplexer coupled to selectively couple an output of a first one of the divide stages to an input of a second one of the divide stages.

13. (Previously presented) The frequency divider of claim 11 further comprising a duty-cycle stage coupled to correct a duty cycle of an output of at least one of the divide stages having an odd divide ratio.

14. (Original) The frequency divider of claim 13, wherein the duty-cycle stage includes:

a first input to receive a first signal having an unbalanced duty cycle;

a second input to receive a second signal, wherein the second signal is a delayed version of the first signal; and

logic to generate a signal having a balanced duty cycle using the first signal and the second signal.

15. (Canceled)

16. (Previously presented) The frequency divider of claim 11 further including self-correction logic coupled to outputs of at least some of the divide stages to correct an abnormal state of the frequency divider.

17. (Previously presented) The frequency divider of claim 16 further including a latch circuit, the latch circuit including:

the self-correction logic; and

selection circuitry implementing a multiplexer.

18. (Canceled)

19. (Original) The frequency divider of claim 11, wherein the plurality of divide stages are programmably coupled to produce an output having a divide ratio selected from the following group of divide ratios: 1/11, 1/9, 1/7, 1/6, 1/5, and 1/4.

20. (Currently amended) A clock generation circuit comprising:

an input coupled to receive a signal having a first frequency;

an output coupled to provide a clock signal having a frequency derived from the first frequency;

a divider coupled to the input and the output, the divider including:

a sequence of synchronous divide stages to provide a plurality of different divide ratios;

one or more multiplexers to selectively feed-back an output of a divide stage to an input of a divide stage earlier in the sequence; and

wherein respective ones of the divide stages are selectively coupled to a power supply node through switches to selectively power divide stages used for a programmed divide ratio and at least other one of the divide stages not used for the programmed divide ratio is decoupled from the power supply node ~~further comprise an activation input coupled to receive an activation signal to selectively turn off respective divide stages if the respective divide stages are not used for a desired divide ratio~~.

21. (Previously presented) The clock generation circuit of claim 20 wherein the divider further includes a duty-cycle stage coupled to correct a duty cycle of an output of one or more of the divider stages having an odd divide ratio.

22. (Original) The clock generation circuit of claim 21, wherein the duty-cycle stage includes:

a first input to receive a first signal having an unbalanced duty cycle;

a second input to receive a second signal, wherein the second signal is a delayed version of the first signal; and

logic to generate a third signal having a balanced duty cycle using the first signal and the second signal.

23. (Canceled)

24. (Previously presented) The clock generation circuit of claim 20 wherein said divider includes self-correction logic coupled to outputs of at least some of the divide stages to correct abnormal states of the divider.

25. (Previously presented) The clock generation circuit of claim 24 wherein said divider further includes a latch circuit in at least one of the divide stages, the latch circuit including:

the self-correction logic; and

selection circuitry implementing at least one of the one or more multiplexers.

26. (Canceled)

27. (Previously presented) A method comprising:

providing an input clock to a divider, the divider including a sequence of divide stages coupled to selectively provide a plurality of different divide ratios;

clocking each of the divide stages with the input clock;

selectively feeding back an output of a first one of the divide stages to an input of a second one of the divide stages earlier in the sequence of divide stages; and

selectively turning off one or more of the divide stages if the one or more divide stages is not used for a desired divide ratio.

28. (Original) The method of claim 27 further comprising programming the divider to produce a selected divide ratio.

29. (Canceled)

30. (Original) The method of claim 27 further comprising correcting a duty cycle of an output produced by the divider.

31. (Previously presented) The method of claim 30, wherein correcting the duty cycle includes:

generating a first signal having an unbalanced duty cycle;

generating a second signal, wherein the second signal is a delayed version of the first signal; and

logically combining the first signal and the second signal to generate an output signal having a balanced duty cycle.

32. (Original) The method of claim 27 further including correcting an abnormal state of one or more divider stages.

33. (Previously presented) The method of claim 32 wherein correcting the abnormal state includes:

latching an output of a selected portion of a correction circuit, wherein the portion is selected based, at least in part, on a divide ratio to be achieved.

34. (Previously presented) A circuit comprising:

means for providing an input clock to a divider, the divider including means for selectively providing a plurality of different divide ratios;

means for clocking each of a plurality of divide stages with the input clock;

means for selectively feeding back an output of at least one of the divide stages to an input of another of the divide stages; and

means for selectively turning off one or more of the stages of the divider if the one or more stages is not used for a desired divide ratio.

35. (Canceled)

36. (Original) The circuit of claim 34 further comprising means for correcting a duty cycle of an output produced by the divider.

37. (Original) The circuit of claim 34 further including means for correcting an abnormal state of one or more stages of the divider.

38. (Original) The circuit of claim 37 wherein the means for correcting an abnormal state includes means for latching an output of a selected portion of a correction circuit, wherein the portion is selected based, at least in part, on a divide ratio to be achieved.

39. (Original) The circuit of claim 34 further comprising means for programming the divider to produce a selected divide ratio.

40. (New) The frequency divider of claim 11 further comprising switches for selectively turning off the one or more divide stages according to whether the one or more divide stages is being used for the programmed divide ratio.

41. (New) The frequency divider of claim 11 further comprising respective switches selectively coupling respective ones of the divide stages to a power supply node according to whether the respective ones of the divide stages are being used for the programmed divide ratio.